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REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability. Accordingly, after the Examiner completes a thorough examination, a Notice of Allowance is respectfully requested in due course. If any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number below.

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~~Electrically erasable and programmable, non-volatile, semiconductor memory device having a single layer of gate material, and corresponding memory plane~~

SUBSTITUTE SPECIFICATION

ELECTRICALLY ERASABLE AND PROGRAMMABLE, NON-VOLATILE, SEMICONDUCTOR MEMORY DEVICE HAVING A SINGLE LAYER OF GATE MATERIAL, AND CORRESPONDING MEMORY PLANE

Field of the Invention

[0001] The present invention relates to integrated circuits and more particularly to semiconductor memory devices of the electrically erasable and programmable, non-volatile type having a single layer of gate material.

Background of the Invention

The structure of ~~such a~~a conventional memory cell is ~~well known to those skilled in the art.~~disclosed, for example, in United States Patent ~~No. 5 761 121 gives an example of~~No. 5,761,121 directed to a memory cell for a PMOS structure. More specifically, such a cell ~~comprises a~~ includes a floating-~~floating~~ gate transistor and a control gate which is produced by implantation within a semiconductor substrate. This buried layer, which acts as control gate is capacitively coupled to the floating gate. The control

gate and the floating-gate transistor are electrically isolated by an isolation zone, for example of the STI (Shallow Trench Isolation) type.

[0002] The layer of gate material, generally made of polysilicon, within which the floating gate of the transistor is produced, is isolated from the active zone by a dielectric, for example, silicon dioxide.

[0003] Although such a memory cell is programmed by injecting hot electrons into the floating gate of the transistor, these being called CHE (Channel Hot Electrons), such a memory cell is electrically erased by applying a high voltage to the source, the drain and the substrate of the transistor and by applying a much lower voltage to the control gate. This induces a high reverse electric field and therefore causes the electrons stored in the floating gate to be extracted and sent into the source, drain and channel regions of the transistor, and by doing so passing through the gate oxide of the transistor.

However, this erase process, when it is repeated in a cyclic fashion, as is generally the case for memory applications, causes the gate oxide of the transistor and the threshold voltage of this transistor to be degraded.

[0004] In other words, repeatedly extracting the electrons through the gate oxide of the transistor eventually causes ~~ageing of the latter.~~ aging of the transistor. This problem needs to be addressed.

~~The aim of the invention is to offer a solution to this problem.~~

Summary of the Invention

[0005] It is an object of the present invention to provide a memory cell structure that avoids the phenomenon of transistor ageing during repeated erase cycles.

[0006] It is also an object of the invention to allow the cell to be programmed either by "hot carrier" programming or by "Fowler-Nordheim" programming.

[0007] It is also an object of the invention to provide such a memory cell whose fabrication process is~~completely~~ compatible with a conventional CMOS fabrication process.

The invention therefore provides a semiconductor memory device comprising an electrically erasable programmable non-volatile memory cell having a single layer of gate material and including a floating-gate transistor and a control~~gate.~~

[0008] gate. According to a general feature of the invention, the source, drain and channel regions of the floating-gate transistor form the control gate. Moreover, the memory cell includes a dielectric zone lying between a first part of the layer of gate material and a first semiconductor active zone electrically isolated from a second active zone incorporating the control gate. This dielectric zone then forms a "tunnel" zone for transferring, during erasure of the cell, the charges stored in the floating gate to the said first active zone.

[0009] The channel region is understood to mean here as being the semiconductor region extending between the source region and the drain region beneath the gate of the transistor.

~~According~~According to the invention, the structure of the memory cell is consequently completely different from the conventional structures in the sense that it has no control gate separate from the floating-gate tran~~sistor.~~sistor. This is because, according to the invention, it is a part of the floating-gate transistor, and more particularly the source, drain and channel regions of this transistor, that form the control~~gate.~~

[0010] gate. Moreover, during erasure of the cell, the charges are extracted no longer through the gate oxide of the floating-gate transistor but through a gate oxide (dielectric) which is located opposite an active zone electrically isolated from the active zone incorporating the control gate, and consequently the source, channel and drain regions of the floating-gate transistor. As a consequence, according to the invention, degradation of the oxide in the tunnel zone does not cause the transistor of the cell to undergo ageing.

[0011] The fact that the source, drain and channel regions of the transistor form the control gate, and that the tunnel zone located opposite the~~said~~ first active zone ~~constitutes~~defines the charge transfer zone, is due to the fact that the capacitive coupling between the second active zone (that in which the

source, drain and channel regions of the transistor are produced) and the floating gate is greater than the capacitive coupling within the tunnel zone. The differences in capacitive coupling depend on the areas of gate material opposite the active zones and on the different voltages applied to the various electrodes of the memory cell. A person skilled in the art will know how to adjust these various parameters~~in order~~ to obtain the desired effect.

[0012] However, to obtain the advantages of the memory cell according to the invention, while still applying reasonable voltages to the electrodes of the memory cell, that is to say voltages from around a few volts to about ten volts, it will be advantageous to choose the capacitance of the tunnel zone to be less than or equal to 30% of the total capacitance between the layer of gate material and all of the active zones of the memory cell.

[0013] According to one embodiment of the invention, the transistor has an annular gate and the layer of gate material includes, in addition to the~~said~~ annular gate and the~~said~~ first part, a linking part between this first part and the annular gate.

Several possibilities exist for the electrical isolation between the first active zone (that into which the charges will be transferred during erasure) and the second active zone (that in which the transistor is produced).

[0014] According to a first embodiment, the first active zone and the second active zone are electrically

isolated from each other by PN junctions intended to be reverse-biased, and on the surface by an isolation region, for example an isolation region of the shallow trench type.

[0015] In this case, and according to one embodiment, the first active zone is produced in a first substrate region (for example a well), having a first type of conductivity, for example, N-type conductivity. The second active zone is produced in a second substrate region (for example a well) also having the first type of conductivity. The first substrate region and the second substrate region are then separated by a third substrate region (for example another well) having a second type of conductivity different from the first, for example P-type conductivity. The isolation region extends between the first substrate region and the second substrate region and then includes an aperture emerging in a contact zone (for example a P^+ zone) in the third semiconductor region.

As a variant, the first active zone and the second active zone may be electrically isolated from each other solely by PN junctions intended to be~~reverse-biased.~~

reverse-biased. Such an embodiment allows better data retention to be obtained. This is because it has been observed that it is necessary to choose a dielectric thickness in excess of 60 Å so as to obtain good data retention. However, it has been observed that thinning of the gate dielectric occurs at the interface between the isolation zone, for example of the shallow trench

type, and the gate material. This leads to inferior data retention. Consequently, the embodiment providing for there to be no overlap of the isolation region by the gate material ~~solves~~addresses this problem.

[0016]

More specifically, according to one embodiment, the layer of gate material extends entirely above the three or four mentioned substrate regions, without overlapping the isolation region.

[0017] Whatever the embodiment, the first substrate region includes, on the surface, a contact zone having the first type of conductivity, for example an N^+-type contact zone in an N well.

This being the case, to facilitate erasure it may prove advantageous to provide, on the surface of the first active zone, in addition to the aforementioned contact, a surface zone having the second type of conductivity, for example P^+-type conductivity, and extending around the~~said~~ tunnel zone. Of course, this surface zone is electrically connected to the contact zone, for example, by siliciding.

[0018] Thus, a transistor, for example a PMOS transistor, whose source and drain regions are short-circuited will be produced with the first part of the gate material. This will allow that part of the active zone located beneath the first part of the gate material to be very conducting.

[0019] It would also be possible not to limit the contact locally, but to produce, on the surface, any highly doped zone having the first type of

conductivity, for example, N^+-type conductivity. Doing so would probably result in perimetric erasure.

According to one embodiment of the invention, the device furthermore includes bias means possessing a memory cell programming state, a memory cell read state and a memory cell erase state.

In the erase state, the bias means cause Fowler-Nordheim erasing by applying a voltage to the first active zone that is much higher than the voltages applied to the source, drain and substrate regions of the~~transistor.~~

[0020] transistor. In this regard, in the erase state, the bias means preferably apply equal voltages to the source, drain and substrate regions of the transistor.

In the programming state, the bias means may cause hot-carrier programming within the transistor. They may also cause Fowler-Nordheim programming, by applying preferably equal voltages to the source, drain and substrate regions of the transistor that are much higher than those applied to the first active zone.

[0021] Moreover, in the read state, it will be advantageous to choose a drain/source voltage difference limited to 1 volt in absolute value. This prevents very slow reprogramming of the memory cell, or else unintentional, parasitic programming of a virgin memory cell.

The floating-gate transistor is preferably a PMOS transistor. However, the invention also applies to an NMOS transistor.

The device may comprise a memory plane made up of several memory~~cells.~~

cells. The device may thus form a memory of the EEPROM type or of the FLASH type.

[0022] The subject of the invention is also an integrated circuit that includes a device as defined above.

Brief Description of the Drawings

[0023] Further advantages and features of the invention will become apparent on examining the detailed description of non-limiting embodiments and the appended drawings in which:

[0024] ~~Figures 1,~~FIG. 1, 1a, 1b~~illustrate~~ diagrammatically illustrate a first embodiment of a memory device according to the ~~invention;~~invention.

[0025] ~~Figures 2, 2a, 2b illustrate~~FIGS. 2, 2a, 2b diagrammatically illustrate a second embodiment of a memory device according to the ~~invention;~~invention.

[0026] ~~Figures 3, 3a, 3b illustrate~~FIGS. 3, 3a, 3b diagrammatically illustrate a third embodiment of a memory device according to the ~~invention;~~invention.

[0027] ~~Figure 4 illustrates~~FIG. 4 diagrammatically illustrates biases applied to the

electrodes of a memory device according to the invention, depending on the state of this ~~device;~~device.

[0028] ~~Figure 5 illustrates~~FIG. 5 diagrammatically illustrates a fourth embodiment of a memory device according to the invention, particularly one intended to be incorporated within a memory ~~plane;~~plane.

[0029] ~~Figure 6~~FIG. 6 illustrates one embodiment of such a memory ~~plane;~~plane.

[0030] ~~Figures 7 and 8 illustrate~~FIGS. 7 and 8 diagrammatically illustrate biases applied to the electrodes of the memory device of Figures 5 and 6, depending on the state of these ~~devices,~~devices.

[0031] ~~Figures 9 to 11 illustrate~~FIGS. 9 to 11 diagrammatically illustrate a variant of the invention, which provides two-step hot-carrier ~~programming;~~ programming.

[0032] ~~Figure 12 illustrates~~FIG. 12 schematically illustrates a fifth embodiment of a memory device according to the invention, particularly one intended to be incorporated within a memory ~~plane;~~plane.

[0033] ~~Figures 13~~FIGS. 13 and 14 illustrate one embodiment of such a memory ~~plane; and~~plane.

[0034] ~~Figure 15 illustrates~~FIG. 15 schematically illustrates the bias voltages applied to the electrodes of the memory device of Figures 12 and 13, depending on the state of these devices.

Detailed Description of the Preferred Embodiments

In the following, Figure 1a (or alternatively 2a and 3a) and Figure 1b (or alternatively 2b and 3b) are

sections on the lines A-A and B-B, respectively, of Figure 1 (or alternatively of Figure 2 and ~~Figure 3.~~ Figure 3).

In Figures 1a and 1b, the reference SB denotes a semiconductor substrate, for example made of P^--doped silicon, of an integrated circuit.

[0035] This substrate SB comprises a first substrate region RG1, formed from an N-doped semiconductor well, and a second substrate region RG2, formed from another N-doped semiconductor well. The two wells RG1 and RG2 are separated by a third semiconductor region RG3 formed from a P-doped well.

The well RG3 provides the mutual electrical isolation, depthwise, of the two wells RG1 and RG2. This electrical isolation is in fact produced by PN junctions that will be reverse-biased.

On the surface, the mutual electrical isolation of the two wells RG1 and RG2 is provided by an isolation region STI (shallow trench~~isolation)~~

isolation). The isolation region STI includes an aperture opening into a P^+-doped contact zone PSB located on the surface of the well RG3. This contact PSB will be used to bias the well RG3 and also the subjacent substrate SB.

[0036] The well RG1 forms a first active zone, while the well RG2 forms a second active zone.

Provided above these two active zones is a layer of a gate material, for example polysilicon, resting via a

gate oxide OX, for example silicon dioxide, on the surface of the two active~~zones.~~

[0037] zones. The layer of gate material, which in its entirety forms a floating gate, includes a first part P1 vertically above the first active zone RG1.

The layer of gate material also includes an annular part FG lying above the second active zone RG2. This annular part of the gate material defines the gate FG of a PMOS transistor, also called a read or charge storage transistor, whose source S, formed from a P^+-type implanted region lies within the well RG2 outside the annular gate and whose drain D, also formed from a P^+-type implanted region, lies within the cell RG2 inside the ring forming the gate FG.

[0038] The layer of gate material also includes a linking part PL connecting the annular part FG to the first part P1.

[0039] The geometry of the first part P1 has been chosen so that the capacitance of the oxide zone OX located beneath this first part P1, ~~said~~the zone also being called the tunnel zone ZTN for reasons that will be explained in greater detail below, is less than or equal to 30% of the total capacitance between the layer of gate material and all of the active zones of the memory cell, that is to say the sum of the capacitances formed between the gate material and each of the active zones of the memory cell.

[0040] In this way, the source, drain and channel regions, which are capacitively coupled to the gate FG,

will form a control gate for this memory cell, while the tunnel zone ZTN will form a charge transfer zone for extracting, during erasure of the memory cell, the charges stored in the floating gate, transferring them to the first active zone RG1.

~~As regards~~Regarding the control gate, it is of course the channel zone which contributes mostly to the capacitive coupling with the annular gate FG. This being so, a person skilled in the art knows that the source and drain regions also extend, by diffusion, under the annular gate FG. The source and drain regions therefore also contribute in practice to this capacitive coupling.

For suitably biasing the first active zone RG1 and for making contact, this zone includes an N^+ implanted zone, with the reference~~PC1.~~

[0041] PC1. Moreover, in this embodiment, a P^+-doped surface zone ZS extending around the tunnel zone ZTN is also provided.

A person skilled in the art will have noted that what has thus been formed with the first part P1 of the layer of gate material is a short-circuited PMOS transistor, that is to say one whose P^+-doped source and drain regions are electrically connected~~together.~~

together. This surface zone ZS is electrically connected to the contact zone PC1, for example by surface~~siliciding.~~

[0042] ~~As regards~~siliciding. Regarding the second active zone RG2, this is also provided with an N^+ implanted region with the reference BK, for contacting and biasing this well RG2, and consequently for biasing a substrate of the read transistor.

The process for fabricating such a memory cell firstly comprises the production in a manner known per se, of the lateral isolation regions STI in the P^--type substrate~~SB.~~

SB. The process then continues, in a manner known per se, with the implantation of the wells RG1, RG2 and RG3.

[0043] After an oxide layer OX has been produced on the surface of the structure thus obtained, a layer of gate material, for example polysilicon, is then deposited, which is etched so as to form in this annular gate layer FG, the linking part PL and the first part P1. Next, the various P^+ and N^+ implanted regions are produced, the layer of gate material then serving especially as hard mask.

A conventional siliciding operation is then carried out on the source, drain and contact regions PC1, BK, and on the surface zone~~ZS.~~

[0044] ZS. The fabrication process is then completed with conventional contacts on the source and drain regions, on the region BK and on the contact PC1.

The operation of the memory cell according to the invention will now be described, more particularly with reference to~~Figure 4.~~

Figure 4. In this regard, the memory device according to the invention includes a bias circuit or means MPL, for example voltage sources associated with a control logic, these bias means possessing a memory cell programming state, a memory cell read state and a memory cell erase state.

[0045] In each of these states the means MPL deliver voltages VS, VD and VBK, to the source S, the drain D and the substrate BK of the transistor. They also bias the substrate RG3 with a voltage VPSB applied to the contact zone PSB and bias the first active zone RG1 with a voltage VZ1 applied to the contact zone PC1.

[0046] Another possibility of electrically programming the memory cell ~~consists in~~includes adopting what is called "hot electron" programming. More specifically, when it is wished to program the memory cell electrically, that is to say when it is wished to store charges in the floating gate, a voltage of 5 volts supplied to the source of the transistor and a voltage of 0 volts is applied to the drain, for example.

[0047] The substrate of the transistor is also biased with 5 volts and a voltage, which may vary in practice between 0 and 5 volts, for example, 5 volts, is applied to the contact PC1 of the first active zone. The substrate (contact PSB) is also biased with 0 volts. The transistor is then in the on state

(provided that there is a sufficient gate/source voltage for making the transistor start to conduct), thereby saturating this transistor and generating a hole current coming from the source. These holes collide with the crystal lattice and form hot holes and hot electrons. The hot electrons are attracted to the floating gate, the potential of which drops slightly with respect to that applied to the source.

Another possible way of programming the memory cell according to the invention ~~consists in~~includes carrying out Fowler-Nordheim programming, that is to say applying a high electric field in order to lower the energy barriers and allow the electrons to flow towards the floating gate.

More specifically in this case, equal voltages will, for example be applied to the source, drain and substrate of the transistor, the value of which is relatively high, for example between 8 and 11 volts, and typically 11 volts. At the same time, while the well RG3 is still biased to 0 volts, a voltage of 0 volts is applied to the contact PC1 of the first active zone.

[0048] In this way, the floating gate is raised to a potential substantially equal to 10 volts, while the first active zone is at 0 volts. This therefore creates a strong electric field which will attract the electrons from the first active zone RG1 to the floating gate through the oxide of the tunnel zone ZTN.

The memory cell according to the invention therefore has the advantage of being able to be programmed in two

different ways, either by hot-electron programming or by Fowler-Nordheim programming. It will thus be possible to choose the type of programming according to the envisaged~~applications.~~

[0049] applications. Hot-electron programming has a higher current consumption, more rapid, however, than Fowler-Nordheim programming, which has a lower consumption. It will therefore be preferable to choose Fowler-Nordheim programming in mobile telephony applications.

In the read state, the drain/source voltage difference is intentionally limited to -1 volt so as to avoid very slow reprogramming of the memory cells. Thus, for example, a voltage of 3.3 volts on the source and a voltage of 2.3 volts on the drain will be chosen. The substrate BK will be biased with 3.3 volts and the control gate (source and drain) may be biased with a voltage varying between 0 and~~3.3 volts.~~

[0050] 3.3 volts. Thus, if during programming a 0 is programmed into the memory cell, that is to say if, in fact, no programming has been carried out, the transistor will be off during reading.

[0051] On the other hand, if in the programming state a "1" (for example) is programmed into the memory cell, that is to say if charges are stored in the floating gate, the transistor will conduct during reading. Thus, by detecting whether or not there is a current in the read state it is possible to determine the logic value that has been written or programmed into the cell.

To erase the memory cell, a voltage is applied to the first active zone that is much higher than those applied to the source, drain and substrate regions of the~~transistor.~~

[0052] transistor. As an indication, a 0 voltage is applied to the source, the substrate and the drain of the transistor and a voltage of, for example, 11 volts is applied to the contact PC1, the substrate RG3 still being biased with 0 volts. This Fowler-Nordheim erasing therefore leads to the application of a very high electric field, the reverse of that for programming, and consequently causes the charges stored in the floating gate to be extracted towards the active zone RG1, via the tunnel ZTN, as far as the contact PC1.

There is therefore no degradation of the oxide of the memory cell's transistor, which corresponds to the zone of highest~~coupling.~~

coupling. In certain cases, the erasure of a memory cell may result in this cell being in an over-erasure state, for example when the erase time is too~~long.~~

long. This over-erasure state is manifested, when the transistor of the cell is a PMOS transistor, by the presence of positive electrical charges in the floating gate of the transistor. This state is illustrated in Figure 9 in terms of the voltage threshold~~VT.~~

[0053] VT. In that figure, the curve VT1 corresponds to a threshold voltage of a PMOS transistor of a

fabrication output cell. Typically, the threshold voltage is around -0.6 volts.

When a cell is programmed by hot electrons, electrons are stored in the floating gate, which shifts the threshold voltage towards positive values, for example to a value of around 1.4 volts (curve VT4). The threshold voltage shift is then around~~2 volts.~~ 2 volts. The purpose of erasing this programmed cell is to bring the threshold voltage of the transistor substantially back to its initial value (curve VT1).

[0054]

[0055] However, in the event of over-erasure, this is manifested by a shift in the threshold voltage towards negative values (for example curve VT2). In this case, it may prove extremely difficult, if not impossible, to reprogram the cell. This is because if the absolute value of the threshold voltage of the transistor remains above the absolute value of the gate-source voltage difference, the transistor of the cell cannot be turned on, therefore preventing the production of hot electrons.

[0056] To remedy this drawback, the biasing means MPL will program a memory cell having undergone an erasure, the transistor of which is a PMOS transistor, by carrying out hot-electron programming of the transistor in two successive steps, so as firstly to compensate for any residual positive charges present in the floating gate and then to perform optimum programming (Figure 10).

More precisely, in the first step, the biasing means MPL compensate for any residual positive charges present in the floating gate by applying a compensation voltage VZ1 to the contact PC1 of the first active ~~zone.~~

[0057] zone. This voltage VZ1 is, for example, equal to 0 volts, but it could also be negative, for example greater than about -500 mV. However, it is necessary to ensure that too negative a compensation voltage is not applied so as not to bring the PN diode formed by the well RG1 and the well RG3 into forward conduction.

Applying this compensation voltage, for example for 500 microseconds, not only makes it possible to compensate for the negative shift of the threshold voltage but also to initiate the hot-electron programming. Thus, at the end of this first step, the threshold voltage is shifted to the right relative to the initial voltage (curve VT3 shifted to the right relative to curve~~VT1).~~

[0058] VT1). The optimum programming is then carried out by applying, for example for 100 microseconds, a voltage VZ1 to the contact PC1 of 5 volts. The threshold voltage is then again shifted to the right (curve VT4).

It will therefore have been noted that this variant of the invention makes it possible to obviate the drawback associated with over-erasure by employing two-step programming using the contact PC1 that is normally used for~~erasure.~~

[0059] erasure. The invention is not limited to the embodiment that has just been described, rather it embraces all variants.

Thus, as illustrated in Figures 2, 2a and 2b, the N^+-doped contact PC1 of the first active zone may extend over the entire surface of this first active zone, except of course beneath the first part P1 of the gate material.

[0060] In this case, since there is no implantation in the linking part PL of the gate material, what is then formed, in the gate material is a PIN diode, that is to say a diode formed from a P^+ region and an N^+ region separated by a region of intrinsic gate material. However, during erasing, this diode is reverse-biased and may somewhat counteract the erasing efficiency. This is the reason why, in some applications, it will be preferred to use the embodiment illustrated in Figures 1, 1a and 1b.

In another embodiment, the contact PC1 may remain localized, and the remainder of the N-doped active zone RG1.

[0061] Another conceivable embodiment is that illustrated in Figures 3, 3a and 3b. It will be seen in these figures that there are no isolation zones STI on the surface between the first active zone and the second active zone. In this case, isolation is achieved only by reverse-biased PN junctions.

In the example illustrated in these figures, the first active zone is an N^+-type implanted surface zone.

However, the N^+ contact could be localized and could also have a P^+ implantation of the surface zone type similar to that illustrated in~~Figures 1.~~

[0062] Figures 1. This embodiment, in which the layer of gate material extends entirely above the active zones of the memory cell without overlapping the lateral isolation region, allows better data retention. This is because the phenomenon of oxide thinning at the interface between an isolation zone and the gate material is thus avoided.

However, it will be necessary in this embodiment to use an appropriate mask during the siliciding step so as not to silicide the floating gate or the PN surface functions, and therefore so as not to create a metal short circuit. Furthermore, the fact of not siliciding the floating gate allows better data~~retention.~~

[0063] retention. Of course, the programming, reading and erasing of the memory cells like those illustrated in Figures 2 and 3 are similar to those described with reference to Figures 1.

Finally, although the electrically erasable programmable non-volatile memory cell that has just been described uses a PMOS transistor, construction based on an NMOS transistor is also~~conceivable.~~

conceivable. Moreover, several memory cells may be provided so as to form a memory plane which can be erasable bit by bit, so as to form a memory of the EEPROM type, or else erasable by bank or by page so as to form a memory of the FLASH type, however, it will

then be necessary to associate an access transistor with each memory cell so as to be able to select~~it.~~

[0064] it. In this regard, the embodiment of the cell illustrated in Figure 5 can be used to produce a memory plane such as that illustrated in Figure 6, offering an architecture of small size with a high cell programming current and good isolation between the lines of bits.

This is obtained according to the invention, especially by the use of an access transistor having a particular shape which will lead to the access transistors of the neighbouring cells being brought into contribution.

More specifically, Figure 5 illustrates a memory cell CEL_i which, assumed here to be flanked by two adjacent memory cells CEL_{i-1} and CEL_{i+1} located in the same column CL_j as the said memory cell (Figure 6), includes an access transistor with the reference $TACS_i$.

[0065] This access transistor $TACS_i$ assigned to the memory cell CEL_i, partially surrounds the floating-gate FG transistor of the memory cell.

More precisely, this access transistor $TACS_i$ may be divided into three elementary access~~transistors.~~

transistors. Thus, a first elementary access transistor $TACSEL1_i$ is specifically associated with the memory cell~~CEL_i.~~

CEL_i. On the other hand, the second elementary access transistor $TACSEL2_i$ and the third elementary access

transistor $TACSEL3_i$ are respectively common to the two access transistors $TACS_{i-1}$ and $TACS_{i+1}$, which are assigned to the two adjacent memory cells CEL_{i-1} and CEL_{i+1}, ~~respectively.~~

respectively. The source of the access transistor $TACS_i$ forms the source of the first elementary access transistor~~$TACSEL1_i$.~~

[0066] $TACSEL1_i$. Moreover, the drain of the first elementary access transistor $TACSEL1_i$ forms part of the source S of the floating-gate transistor FG of the memory cell.

Referring now more particularly to Figure 6, which shows the memory plane formed from the cells illustrated in Figure 5, it may be seen that each memory cell column, for example the column CL_j includes a layer of gate material MTL_j possessing a principal part PMTL extending in the direction of the column along and facing all the floating-gate transistors FG of the cells.

[0067] The gate $GREL1_i$ of the first elementary transistor $TACSEL1_i$ of the access transistor $TACS_i$ then includes that portion of the said principal part of the layer of gate material MTL_j which is located opposite the~~floating~~ floating-gate transistor FG of the cell CEL_i.

Moreover, this layer of gate material MTL_j includes, at each memory cell, for example at the memory cell CEL_i, a second elementary portion $E2MTL_j$ connected to the principal part $PMTL_j$ and extending approximately

perpendicular to this principal part on one side of the floating-gate~~transistor.~~

[0068] transistor. This second elementary portion $E2MTL_j$ then forms part of the gate $GREL2_i$ of the second elementary transistor $TACSEL2_i$.

The layer of gate material MTL_j also includes a third elementary portion $E3NMTL_j$, which is also connected to the principal part $PMTL_j$ and extends approximately perpendicular to this principal part on the other side of the floating-gate transistor of the cell~~CEL_i.~~

[0069] CEL_i. This third elementary portion $E3MTL_j$ forms part of the gate $GREL3_i$ of the third elementary transistor $TACSEL3_i$.

Figure 6 also shows that the second elementary portion $E2MTL_j$ associated with a memory cell forms the third elementary portion associated with one of the two adjacent memory cells, while the third elementary portion $E3MTL_j$ associated with the memory cell CEL_i forms the second elementary portion associated with the other of the adjacent memory~~cells.~~

[0070] cells. The source of each access transistor $TACS_i$ includes a plurality of contacts SLC which are all connected together by means of the same metallization.

So as to further increase the current of the access transistor when the latter is on, other contacts SLC are placed externally near the ends of the gates $GREL2_i$ and $GREL3_i$ of the other two elementary access ~~transistors.~~

transistors. Moreover, the drain contacts BLC of the memory cells of any one line are connected together and consequently form a bit~~line.~~

line. The layer of gate material MTL_j of each column is also intended to be biased by a gate bias voltage, and the metallization for taking the gate bias voltage on to the layer MTL_j forms a column metallization (row~~line).~~

[0071] line). It should therefore be pointed out here that there is no specific contact on the source S of the floating-gate transistor of a memory cell. This source is consequently floating.

The operation of the memory plane will now be described more particularly, also with reference to Figures 7 and~~8.~~

8. In general, the memory device according to the invention includes bias means MPL2 capable of selecting at least one memory cell in programming mode and in read mode and capable of erasing the memory plane by blocks of cells, in this case here by two columns simultaneously.

This is because it may be seen in Figure 6 that all the contacts PC1 of the memory cells of two adjacent columns CL_j and CL_{j+1} are connected together by the same metallization MTL2.

[0072] On the other hand, in programming or read mode, it will if necessary be possible to select only a

single cell at a time by varying the bias of the lines of bits and of the column metallizations (row lines).

It is apparent from the architecture illustrated in Figure 6 that the bias means are consequently capable of applying the same source bias voltage to the respective sources SLC of the access transistors assigned to the memory cells of the same column, ~~respectively.~~

respectively. Moreover, these bias means MPL2 may apply the same gate bias voltage to the respective gates of the access transistors assigned to the memory cells of any one column~~respectively.~~

[0073] respectively. Finally, as indicated above, the bias means may apply the same erase voltage to the respective first active zones RG1 of the memory cells of at least any one column, and in this case in particular of two adjacent columns.

In a manner similar to what has been described in the case of the embodiments illustrated in Figures 1 to 3, the bias means MPL2 possess a programming state in which they are capable of programming a memory cell. They also possess a read state in which they are capable of reading a memory cell. Furthermore, they possess an erase state in which they are capable of erasing at least one column of memory~~cells.~~

[0074] cells. In each of these states, the bias means are capable of applying predetermined voltages to the sources and the gates of the access transistors, and to the drains and the substrates of the floating-

gate transistors of the cells, and to the first active zones RG1.

We now consider the case in which it is desired to access the cell CEL_{ij}, this cell belonging to the line i and to the column j~~(Figure 7).~~

(Figure 7). In general, to access a memory cell in read mode or programming mode, the bias means MPL2 turn on the access transistors of the memory cells belonging to the same column as that of the memory cell in~~question.~~

question. Moreover, the bias means apply an identical voltage to the source of the access transistor and the drain of the floating-gate transistor of each memory cell of the said column, different from the memory cell in question, so that the other memory cells of the column are not~~affected.~~

[0075] affected. Finally, the bias means MPL2 can turn off the access transistors of the memory cells belonging to a column other than that of the memory cell in question.

As an example, as illustrated in Figure 7, in order to program the cell CEL_{ij} the bias means MPL2 apply, for example, a voltage VMTL = 1.7 volts to the layer of gate material MTL_j of the column~~CL_j.~~

CL_j. Moreover, they apply a voltage VLC, equal to 5 volts, for example, to all the source contacts SLC. Consequently, the gate/source voltage difference of all the access transistors of all the cells of the column

CL_j is equal to -3.3 volts, which consequently turns on all these access~~transistors.~~

[0076] transistors. The bias means MPL2 then apply a voltage VBL equal to 0 volts to the contact BLC (bit line) and they apply voltages VBK, VPSB and VZ1, equal to 5 volts, 0 volts and 5 volts respectively, to the contacts BK, PSB and PC1, respectively.

The cell is then programmed by hot electrons.

[0077] In this regard, it should be noted here, that the invention is noteworthy in the sense that, since the layer of gate material MTL_j forms an equipotential, all the access transistors, that is to say all the elementary access transistors, are on and contribute to delivering the programming current to the cell in question. Of course, the predominant contribution is provided by the access transistor of the cell and the contribution of an access transistor is smaller the further away this access transistor is from the memory cell to which access is made.

[0078] Of course, since it is desirable to access only a single cell of this column and since all the access transistors of the cells of this column are on, it is then necessary, so as not to affect the other cells CEL_{mj} (m different from i) of the same column, to apply equal voltages to the contacts BLC and SLC of these memory cells. In other words, since in the present case the voltage VSLC is fixed at 5 volts, a voltage of 5 volts will be applied to the drains (bit line) of the other cells of the column.

~~As regards~~Regarding the cells CEL_{mn} (n different from j), that is to say the cells belonging to the columns other than the column that includes the cell to which access is made, the bias means MPL2 apply a voltage VMTL equal to the voltage VSLC to the gates of the access transistors MTL_n. Thus, all the access transistors of the cells of these other columns are off, since the gate/source voltage difference is~~zero.~~

[0079] zero. It should be noted here that very good isolation between two neighbouring bit lines is achieved.

If it is now desired to access the cell CEL_{ij} in read mode, the bias means MPL2 apply a voltage equal to 0 volts to the gates of the access transistors and a voltage equal to 3.3 volts to the sources of the access transistors, so as to turn on the access transistors of the cells of the~~columns.~~

[0080] columns. In this read state, the drain/source voltage difference of the floating-gate transistor is intentionally limited to -1 volt so as to avoid very slow reprogramming of the memory cell. A voltage on the drain of 2.3 volts will then be chosen. The substrate BK will be biased with 3.3 volts. In addition, for example, the contact PSB will be earthed and 3.3 volts applied to the contact PC1.

[0081] The erasing of the cells of two neighbouring columns is of the Fowler-Nordheim type. More specifically, in this erase state, the bias means cause Fowler-Nordheim erasing by applying a voltage to the first active zones RG1 which is much higher than that

applied to the source regions of the access transistors and to the drain and substrate regions of the floating-gate transistors.

Thus, as an indication, as illustrated in Figure 8, the bias means MPL2 may apply a voltage VZ1 of 11 volts to the contact PC1, while all the other contacts will ~~beearthed.~~

[0082] earthed. It should be noted here that the fact that the source of the floating-gate transistor of the memory cell is itself floating is compatible with Fowler-Nordheim erasing via the first active zone RG1. This is because the floating source of the transistor is earthed by the memory location itself.

Of course, in the variant illustrated in Figures 5 and 6, an isolation of the type illustrated in Figures 1, 2 and 3 will be used to mutually isolate the various active regions RG1, RG2 and RG3 of the memory location.

[0083] Moreover, two-step hot-electron programming of the cells, as described with reference to Figures 1, 2, 3, 9 and 10, may also be applied to the memory plane of Figure 6. More precisely as illustrated in Figure 11, the bias means MPL2 would then apply in this case, for programming the cell CEL_{ij}, firstly a zero voltage VZ1 to the contact PC1 via the metallization $MTLPC_{i,j+1}$ (figure 6) and an optimum voltage VZ1 of 5 volts.

A fifth embodiment of a memory cell according to the invention, allowing the production of a memory plane requiring less consumption for the programming phase,

thereby making it particularly advantageous for mobile telephone applications for example, will now be described with reference more particularly to Figure 12 *et~~seq.~~*

[0084] *seq.* In Figure 12, the access transistor $TACS_i$ assigned to a memory cell CEL_{ij} comprises a grid $GRTACS_i$ extending perpendicular to the~~said~~ linking part PL and on the opposite side from this linking part with respect to the annular gate FG.

The source of the access transistor comprises a source contact BL_j. The drain of the access transistor forms part of the source S of the floating-gate transistor of the memory~~cell.~~

[0085] cell. The drain of the floating-~~floating~~ gate transistor is electrically connected to the second active zone RG2, that is to say to its substrate (or bulk). The drain zone has in fact a contact WLP_i connected via a metallization (not shown in Figure 12, but illustrated schematically in Figure 13), to the bulk contact BK_i.

As illustrated in Figures 13 and 14, all the source contacts of the access transistors of the cells of any one column j of the memory plane are connected together via a column metallization (bit line), in this case~~BL_j.~~

BL_j. All the first active zones of the cells of any one column j of the memory plane are connected together via their $PC1_j$ and via another column metallization~~VER_j.~~

VER_j. All the drain contacts, and consequently all the bulk contacts of the floating-gate transistors of the cells of any one line i, are connected together via a line metallization~~WLP_i~~.

WLP_i. The gates $GRTACS_i$ of the access transistors of the cells of any one line i of the memory plane are connected together and the corresponding contacts WL_i are also connected together via a line metallization~~WL_i~~.

[0086] WL_i. The memory device furthermore includes bias means MPL3 (figure 15) capable of selecting at least one memory cell in programming mode and of programming it by Fowler-Nordheim programming.

More precisely, in this embodiment, the bias means are capable of selecting a cell of the memory plane and of programming it by applying a sufficient potential difference between the drain of the floating-gate transistor of the cell and the first active zone of this~~cell~~.

[0087] cell. It is therefore not via the access transistor that a cell is selected in programming.

An example of the voltages delivered by the bias means MPL3 and applied to the various metallizations of the memory plane is illustrated in Figure 15 in conjunction with~~Figure 13~~.

Figure 13. More precisely, the configuration 1 of the table given in the top part of Figure 15 corresponds to

a selection and programming of the cell CEL_{11} of Figure13.

13. This example assumes that the supply voltage VPP of the integrated circuit is equal to 6.6 volts, since the oxide thickness of the transistors of the cells is around5 nanometres.

5 nanometres. This voltage VPP is applied to the metallizations WL1 and WLP1 , while the voltage VPP/2 is applied to the metallizations BL1, BL2, WLP2 andVER2.

[0088] VER2. Finally, the metallizations VER1 and WL2 are earthed.

It therefore follows that the access transistor $TACS_1$ of the cell CEL_{11} is off and that the potential of the source of the floating-gate transistor also rises to the voltage VPP by coupling, given that the drain and the substrate are at thispotential.

[0089] potential. Since there then exists a large potential difference (typically 5.6 volts) between the floating gate and the contact $PC1_1$, the cell is programmed by Fowler-Nordheim programming.

However, owing to the application of the voltage VPP/2 to the metallization VER2, there is no sufficient potential difference between the drain of the floating-gate transistor of the cell CEL_{12} and its contact $PC1_2$, and consequently between the floating gate and the contact $PC1_2$. The conditions for Fowler-Nordheim programming are therefore notmet.

met. The conditions for Fowler-Nordheim programming are also not met in the case of the cells CEL_{21} and~~CEL_{22}.~~

[0090] CEL_{22}. The bias means MPL3 are also capable of erasing the memory plane in its entirety, for example by applying a high voltage to all the first active zones of all the cells and by applying a zero voltage to the other contacts of the cells.

In this regard, they apply for example, as indicated in the configuration 2 of the table in Figure 15, a zero voltage to the metallizations BL1, WL1, WLP1, BL2, WL2 and WLP2 and the voltage VPP to the metallizations VER1 and VER2. A Fowler-Nordheim erasing is therefore carried~~out.~~

out. It should be noted here that, as in the variant illustrated in Figures 5 and 6, the fact that the source of the floating-gate transistor of the memory cell is itself floating, is compatible with Fowler-Nordheim erasing via the first active zone RG1. This is because the floating gate of the transistor is taken to earth via the memory location~~itself.~~

[0091] itself. The bias means MPL3 are also capable of reading the memory plane line by line, by turning on the access transistors of the cells of one line and turning off the access transistors of the cells of the other lines.

An example of the voltages applied is indicated in the configuration 3 of the table in~~Figure 15.~~

Figure 15. Throughout all that has just been described in relation to Figures 12 to 15, the bias means MPL3 deliver a zero voltage VPSB to the substrate contact~~PSB.~~

[0092] PSB. Of course, in the variant illustrated in Figures 12 and 14, it would be possible to use an isolation of the type of that illustrated in Figures 1, 2 and 3 in order to mutually isolate the various active regions RG1, RG2 and RG3 of the memory location.

~~CLAIMS~~

THAT WHICH IS CLAIMED IS:

1. Semiconductor memory device comprising an electrically erasable and programmable non-volatile memory cell having a single layer of gate material and including a floating-gate transistor and a control gate, characterized in that the source (S), drain (D) and channel regions of the floating-gate transistor form the control gate and in that the memory cell includes a dielectric zone (ZTN) lying between a first part (P1) of the layer of gate material and a first semiconductor active zone (RG1) electrically isolated from a second active zone (RG2) incorporating the control gate, this dielectric zone forming a tunnel zone (ZTN) for transferring, during erasure of the cell, the charges stored in the floating gate to the said first active zone.

~~2. Device according to Claim 1, characterized in that the capacitance of the tunnel zone (ZTN) is less than or equal to 30% of the total capacitance between the layer of gate material and all of the active zones of the memory cell.~~

~~3. Device according to Claim 1 or 2, characterized in that the transistor has an annular gate (FG) and in that the layer of gate material includes, in addition to the said annular gate (FG) and the said first part (P1), a linking part (PL) between this first part and the annular gate.~~

~~4. Device according to one of the preceding claims, characterized in that the first active zone (RG1) and~~

~~the second active zone (RG2) are electrically isolated from each other by PN junctions intended to be reverse-biased.~~

~~5. Device according to Claim 4, characterized in that the first active zone (RG1) and the second active zone (RG2) are electrically isolated from each other on the surface by an isolation region (STI).~~

~~6. Device according to Claim 5, characterized in that the first active zone (RG1) produced in a first substrate region (RG1) having a first type of conductivity, in that the second active zone is produced in a second substrate region (RG2) also having the first type of conductivity, in that the first substrate region and the second substrate region are separated by a third substrate region (RG3) having a second type of conductivity, different from the first, and in that the isolation region extends between the first substrate region and the second substrate region and includes an aperture emerging in a contact zone (PSB) in the third semiconductor region.~~

~~7. Device according to Claim 4, characterized in that the first active zone (RG1) produced in a first substrate region (RG1) having a first type of conductivity, in that the second active zone is produced in a second substrate region (RG2) also having the first type of conductivity, in that the first substrate region and the second substrate region are separated by a third substrate region (RG3) having a second type of conductivity, different from the first, and in that the layer of gate material (FG, P1, P2)~~

extends entirely above the three substrate regions without overlapping the isolation region (STI).

8. Device according to Claim 6 or 7, characterized in that the first substrate region (RG1) includes, on the surface, a contact zone (PC1) having the first type of conductivity.

9. Device according to Claim 8, characterized in that the first substrate region (RG1) furthermore includes a surface zone (ZS) having the second type of conductivity and extending around the said tunnel zone, this surface zone (ZS) being electrically connected to the said contact zone (PC1).

10. Device according to one of the preceding claims, characterized in that the transistor is a PMOS transistor.

11. Device according to one of the preceding claims, characterized in that it comprises a memory plane having several memory cells, each memory cell being assigned to an access transistor.

12. Device according to one of the preceding claims, characterized in that it furthermore includes bias means (MPL) possessing a memory cell programming state, a memory cell read state and a memory cell erase state, in that the bias means are capable of applying, in each of the states, predetermined voltages to the source, the drain and the substrate of the transistor and to the first active zone and in that, in the erase state, the bias means cause Fowler Nordheim erasing by applying a voltage to the first active zone much higher

than those applied to the source, drain and substrate regions of the transistor.

13. Device according to Claim 12, characterized in that, in the erase state, the bias means (MPL) apply equal voltages to the source, drain and substrate regions of the transistor.

14. Device according to either of Claims 12 and 13, characterized in that, in the programming state, the bias means (MPL) cause hot-carrier programming within the transistor.

15. Device according to either of Claims 12 and 13, characterized in that, in the programming state, the bias means (MPL) cause Fowler-Nordheim programming by applying equal voltages to the source, drain and substrate regions of the transistor that are much higher than that applied to the first active zone.

16. Device according to one of Claims 12 to 15, characterized in that, in the read state, the drain/source voltage difference is limited to 1 volt in absolute value.

17. Device according to Claim 11, characterized in that the access transistor ($TACS_i$) assigned to a memory cell flanked by two adjacent memory cells that are located in the same column as the said memory cell in question includes a first elementary access transistor ($TACSEL1_i$) specifically associated with the said memory cell and second ($TACSEL2_i$) and third ($TACSEL3_i$) elementary access transistors respectively common to the two access transistors assigned to the two adjacent

memory cells respectively, in that the source (SLC) of the access transistor ($TACS_i$) forms the source of the first elementary access transistor while the drain of the first elementary access transistor forms part of the source of the floating gate transistor of the memory cell and in that the device furthermore includes bias means (MPL2) capable of selecting at least one memory cell in program mode and in read mode and of erasing the memory plane by blocks of cells.

18. Device according to Claim 17, characterized in that the bias means (MPL2) are capable of applying the same source bias voltage to the respective sources of the access transistors assigned to the memory cells of any one column respectively, the same gate bias voltage to the respective gates of the access transistors assigned to the memory cells of the same column respectively and the same erase voltage to the respective first active zones of the memory cells of at least the same column.

19. Device according to Claim 17 or 18, characterized in that the access transistor ($TACS_i$) assigned to a memory cell partially surrounds the floating gate transistor of the memory cell.

20. Device according to Claim 19, characterized in that each column (CL_j) of memory cells has a layer of gate material (MTL_j) possessing a main part ($PMTL_j$) extending in the direction of the column along and opposite all the floating gate transistors of the cells, in that the gate of the first elementary transistor of an access transistor assigned to a memory cell includes that portion of the said main part of the

layer of gate material which is located opposite the floating gate transistor of the said cell, in that the layer of gate material includes, within each memory cell, a second, elementary portion ($E2MTL_j$) connected to the principal part and extending approximately perpendicular to this principal part on one side of the floating gate transistor of the cell, so as to form part of the gate of the second elementary transistor of the access transistor, and a third, elementary portion ($E3MTL_j$) connected to the principal part and extending approximately perpendicular to this principal part on the other side of the floating gate transistor of the cell, so as to form part of the gate of the third elementary transistor of the access transistor, and in that the said second elementary portion associated with a memory cell forms the third elementary portion associated with one of the two adjacent memory cells, whereas the said third elementary portion associated with the memory cell forms the second elementary portion associated with the other of the two adjacent memory cells.

21. Device according to one of Claims 17 to 20, characterized in that the bias means (MPL2) possess a programming state in which they are capable of programming a memory cell, a read state in which they are capable of reading a memory cell and an erase state in which they are capable of erasing at least one column of memory cells, in that the bias means are capable of applying, in each of the states, predetermined voltages to the sources and the gates of the access transistors, and to the drains and the substrates of the floating gate transistors of the cells and to the first active zones, and in that, in

~~the erase state, the bias means cause Fowler-Nordheim erasing by applying a voltage to the first active zones that is much higher than those applied to the source regions of the access transistors, and to the drain and substrate regions of the floating gate transistors.~~

~~22. Device according to Claim 21, characterized in that, to access a memory cell in read mode or in programming mode, the bias means (MPL2) turn on the access transistors of the memory cells belonging to the same column as that of the memory cell in question, apply an identical voltage to the source of the access transistor and the drain of the floating gate transistor of each memory cell of the said column different from the memory cell in question and turn off the access transistors of the memory cells belonging to a column other than that of the memory cell in question.~~

~~23. Device according to Claim 14 or either of Claims 21 or 22, characterized in that the bias means (MPL; MPL2) are capable of programming a memory cell that has undergone erasure, the transistor of which cell is a PMOS transistor, by carrying out hot-electron programming on the transistor in two successive steps (PC1 = 0 V; PC1 = 5 V) so as firstly to compensate for any residual positive charges present in the floating gate and then to carry out optimum programming.~~

~~24. Device according to Claim 23, characterized in that, in the first step, the bias means (MPL1; MPL2) compensate for any residual positive charges present in the floating gate by applying a compensation voltage (VZ1) to the contact (PC1) of the first active zone.~~

~~25. Device according to Claim 24, characterized in that the compensation voltage (VZ1) is less than or equal to 0 volts and greater than about -500 mV.~~

~~26.~~ 2. Device according to Claim 1, characterized in that the capacitance of the tunnel zone (ZTN) is less than or equal to 30% of the total capacitance between the layer of gate material and all of the active zones of the memory cell.

3. Device according to Claim 1 or 2, characterized in that the transistor has an annular gate (FG) and in that the layer of gate material includes, in addition to the said annular gate (FG) and the said first part (P1), a linking part (PL) between this first part and the annular gate.

4. Device according to one of the preceding claims, characterized in that the first active zone (RG1) and the second active zone (RG2) are electrically isolated from each other by PN junctions intended to be reverse-biased.

5. Device according to Claim 4, characterized in that the first active zone (RG1) and the second active zone (RG2) are electrically isolated from each other on the surface by an isolation region (STI).

6. Device according to Claim 5, characterized in that the first active zone (RG1) produced in a first substrate region (RG1) having a first type of conductivity, in that the second active

zone is produced in a second substrate region (RG2) also having the first type of conductivity, in that the first substrate region and the second substrate region are separated by a third substrate region (RG3) having a second type of conductivity, different from the first, and in that the isolation region extends between the first substrate region and the second substrate region and includes an aperture emerging in a contact zone (PSB) in the third semiconductor region.

7. Device according to Claim 4, characterized in that the first active zone (RG1) produced in a first substrate region (RG1) having a first type of conductivity, in that the second active zone is produced in a second substrate region (RG2) also having the first type of conductivity, in that the first substrate region and the second substrate region are separated by a third substrate region (RG3) having a second type of conductivity, different from the first, and in that the layer of gate material (FG, P1, P2) extends entirely above the three substrate regions without overlapping the isolation region (STI).

8. Device according to Claim 6 or 7, characterized in that the first substrate region (RG1) includes, on the surface, a contact zone (PC1) having the first type of conductivity.

9. Device according to Claim 8, characterized in that the first substrate region (RG1) furthermore includes a surface zone (ZS) having the second type of conductivity and extending around the said tunnel zone, this surface zone (ZS) being electrically connected to the said contact zone (PC1).

10. Device according to one of the preceding claims, characterized in that the transistor is a PMOS transistor.

11. Device according to one of the preceding claims, characterized in that it comprises a memory plane having several memory cells, each memory cell being assigned to an access transistor.

12. Device according to one of the preceding claims, characterized in that it furthermore includes bias means (MPL) possessing a memory cell programming state, a memory cell read state and a memory cell erase state, in that the bias means are capable of applying, in each of the states, predetermined voltages to the source, the drain and the substrate of the transistor and to the first active zone and in that, in the erase state, the bias means cause Fowler-Nordheim erasing by applying a voltage to the first active zone much higher than those applied to the source, drain and substrate regions of the transistor.

13. Device according to Claim 12, characterized in that, in the erase state, the bias means (MPL) apply equal voltages to the source, drain and substrate regions of the transistor.

14. Device according to either of Claims 12 and 13, characterized in that, in the programming state, the bias means (MPL) cause hot-carrier programming within the transistor.

15. Device according to either of Claims 12 and 13, characterized in that, in the programming state, the bias means (MPL) cause Fowler-Nordheim programming by applying equal voltages to the source, drain and substrate regions of the transistor that are much higher than that applied to the first active zone.

16. Device according to one of Claims 12 to 15, characterized in that, in the read state, the drain/source voltage difference is limited to 1 volt in absolute value.

17. Device according to Claim 11, characterized in that the access transistor ($TACS_i$) assigned to a memory cell flanked by two adjacent memory cells that are located in the same column as the said memory cell in question includes a first elementary access transistor ($TACSEL1_i$) specifically associated with the said memory cell and second ($TACSEL2_i$) and third ($TACSEL3_i$) elementary access transistors respectively common to the two access transistors assigned to the two adjacent memory cells respectively, in that the source (SLC) of the access transistor ($TACS_i$) forms the source of the first elementary access transistor while the drain of the first elementary access transistor forms part of the source of the floating-gate transistor of the memory cell and in that the device furthermore includes bias means (MPL2) capable of selecting at least one memory cell in program mode and in read mode and of erasing the memory plane by blocks of cells.

18. Device according to Claim 17, characterized in that the bias means (MPL2) are capable

of applying the same source bias voltage to the respective sources of the access transistors assigned to the memory cells of any one column respectively, the same gate bias voltage to the respective gates of the access transistors assigned to the memory cells of the same column respectively and the same erase voltage to the respective first active zones of the memory cells of at least the same column.

19. Device according to Claim 17 or 18, characterized in that the access transistor ($TACS_i$) assigned to a memory cell partially surrounds the floating gate transistor of the memory cell.

20. Device according to Claim 19, characterized in that each column (CL_j) of memory cells has a layer of gate material (MTL_j) possessing a main part ($PMTL_j$) extending in the direction of the column along and opposite all the floating-gate transistors of the cells, in that the gate of the first elementary transistor of an access transistor assigned to a memory cell includes that portion of the said main part of the layer of gate material which is located opposite the floating-gate transistor of the said cell, in that the layer of gate material includes, within each memory cell, a second, elementary portion ($E2MTL_j$) connected to the principal part and extending approximately perpendicular to this principal part on one side of the floating-gate transistor of the cell, so as to form part of the gate of the second elementary transistor of the access transistor, and a third, elementary portion ($E3MTL_j$) connected to the principal part and extending approximately perpendicular to this principal part on the other side of the floating-gate transistor of the

cell, so as to form part of the gate of the third elementary transistor of the access transistor, and in that the said second elementary portion associated with a memory cell forms the third elementary portion associated with one of the two adjacent memory cells, whereas the said third elementary portion associated with the memory cell forms the second elementary portion associated with the other of the two adjacent memory cells.

21. Device according to one of Claims 17 to 20, characterized in that the bias means (MPL2) possess a programming state in which they are capable of programming a memory cell, a read state in which they are capable of reading a memory cell and an erase state in which they are capable of erasing at least one column of memory cells, in that the bias means are capable of applying, in each of the states, predetermined voltages to the sources and the gates of the access transistors, and to the drains and the substrates of the floating-gate transistors of the cells and to the first active zones, and in that, in the erase state, the bias means cause Fowler-Nordheim erasing by applying a voltage to the first active zones that is much higher than those applied to the source regions of the access transistors, and to the drain and substrate regions of the floating-gate transistors.

22. Device according to Claim 21, characterized in that, to access a memory cell in read mode or in programming mode, the bias means (MPL2) turn on the access transistors of the memory cells belonging to the same column as that of the memory cell in question, apply an identical voltage to the source of

the access transistor and the drain of the floating-gate transistor of each memory cell of the said column different from the memory cell in question and turn off the access transistors of the memory cells belonging to a column other than that of the memory cell in question.

23. Device according to Claim 14 or either of Claims 21 or 22, characterized in that the bias means (MPL; MPL2) are capable of programming a memory cell that has undergone erasure, the transistor of which cell is a PMOS transistor, by carrying out hot-electron programming on the transistor in two successive steps (PC1 = 0 V; PC1 = 5 V) so as firstly to compensate for any residual positive charges present in the floating gate and then to carry out optimum programming.

24. Device according to Claim 23, characterized in that, in the first step, the bias means (MPL1; MPL2) compensate for any residual positive charges present in the floating gate by applying a compensation voltage (VZ1) to the contact (PC1) of the first active zone.

25. Device according to Claim 24, characterized in that the compensation voltage (VZ1) is less than or equal to 0 volts and greater than about -500 mV.

26. Device according to Claim 3 and 11, characterized in that the access transistor ($TACS_i$) assigned to a memory cell comprises a gate ($GRTACS_i$) extending perpendicular to the said linking part (PL)

and on the opposite side from this linking part with respect to the annular gate, in that the source of the access transistor comprises a source contact (BL_j), in that the drain of the access transistor forms part of the source of the floating-gate transistor of the memory cell and in that the drain of the floating-gate transistor is electrically connected to the second active zone (RG2).

27. Device according to Claim 26, characterized in that all the source contacts of the access transistors of the cells of any one column of the memory plane are connected together (BL1), in that all the first active zones of the cells of any one column of the memory plane are connected together (VER1), in that the gates of the access transistors of the cells of any one line of the memory plane are connected together and the corresponding gate contacts (WLi) are connected together by a line metallization (WL1), in that the drains of the floating-gate transistors of the cells of any one line of the memory plane are connected together in order to form another line metallization (WLP1) and in that the device furthermore includes bias means (MPL3) capable of selecting at least one memory cell in programming mode and of programming it by Fowler-Nordheim programming.

28. Device according to Claim 27, characterized in that the bias means (MPL3) are capable of selecting a cell of the memory plane and of programming it by applying a sufficient potential difference between the drain of the floating-gate transistor of the cell and the first active zone of this cell.

29. Device according to Claim 27 or 28, characterized in that the bias means (MPL3) are capable of erasing the memory plane in its entirety.

30. Device according to Claim 29, characterized in that the bias means (MP3) are capable of erasing the memory plane in its entirety by applying a high voltage to all the first active zones of all the cells and by applying a zero voltage to the other contacts of the cells.

31. Device according to one of Claims 27 to 30, characterized in that the bias means (MPL3) are capable of reading the memory plane line by line by turning on the access transistors of the cell of a line and by turning off the access transistors of the cells of the other lines.

32. Device according to one of the preceding claims, characterized in that it forms a memory of the EEPROM type or the FLASH type.

33. Integrated circuit, characterized in that it includes a device according to one of Claims 1 to 32.